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**COMMUNICATION INTERFACE BETWEEN DISSIMILAR  
PORTS AVOIDING LEVEL TRANSLATION**

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**BACKGROUND OF THE INVENTION**

1. FIELD OF THE INVENTION

15           The present invention relates to a  
communications circuit, and in particular, to an  
interface circuit permitting communication between  
circuits utilizing dissimilar logic families without  
requiring level translation.

20       2. DESCRIPTION OF THE RELATED ART

          The Electronic Industry Association (EIA) and  
the Telecommunications Industry Association (TIA) are  
industry trade associations that have developed  
standards to simplify data communications. The  
25       TIA/EIA-232 (RS232) is one of the oldest and most  
widely known communication standards. It describes  
an unbalanced, unidirectional, point-to point  
interface. The RS232 communication standard has  
periodically been updated, with the latest revision  
30       being RS232-G.

The RS232 standard recognizes differential voltage signals ranging from -12V to +12V. At the time of adoption of the RS232 standard, the  $\pm 12V$  range provided a voltage spectrum broad enough to permit a variety of analog functions to be performed while the resulting signal remained comfortably above background noise. Of course, RS232 circuits were also utilized in digital applications, and an RS232 truth table is given below in TABLE A:

TABLE A  
RS232 Truth Table

VOLTAGE	LOGIC STATE
+3V to +12V	low (=0)
-3V to -12V	high (=1)

While the RS232 standard was once prevalent, over time the widespread use of digital technology dictated the implementation of logic families having voltage ranges different than that of the RS232. For example, reduced voltage ranges became available due to improvement in hardware having reduced background noise levels. Lower voltage ranges were also useful in preserving the thin and fragile gate dielectric structures of MOS devices increasingly employed in digital applications.

Accordingly, more recently implemented logic families utilize a narrower, single-ended voltage range. Voltage signals in these logic families are compatible with the requirements of MOS transistor operation, and reflect reduced noise levels typically encountered in existing digital technology. One such logic family is the transistor-transistor-logic

family (TTL). A truth table for TTL is shown below in TABLE B:

TABLE B  
TTL Truth Table

VOLTAGE	LOGIC STATE
0V to +0.8V	low (=0)
+2.4V to +5.0V	high (=1)

In recent years, several factors have prompted adoption of logic families featuring even narrower voltage ranges than the TTL logic family. One factor is an increased emphasis on portable applications requiring reduced power consumption in order to conserve battery life. Another factor is the ever-shrinking size of MOS devices and the corresponding need to preserve the integrity of thin gate dielectric structures in the presence of applied voltages.

While technology is evolving away from the RS232 communications standard, this standard is still employed in a wide variety of applications. Therefore, there is a need in the art for an interface circuit permitting communication to occur between devices utilizing the RS232 standard and devices utilizing the various other logic families.

FIG. 1 shows a schematic diagram of a conventional interface circuit positioned between a host device featuring an RS232 port, and a peripheral device controlled by a microcontroller utilizing the TTL logic family. Communication circuit 100 includes host device 101 featuring RS232 port 102 having transmit data (TXD) pin 104 and receive data (RXD)

pin 106. TXD pin 104 and RXD pin 106 emit and receive, respectively, signals in which between +3V and +12V are interpreted as a logical low state (=0) and between -3V and -12V are interpreted as a logical high state (=1).

TTL microcontroller 107 of peripheral device 108 features eight pin parallel port 109. Pins 110 of port 109 emit and receive respectively, voltage signals where between 0V and +0.8V represents a logical low state (=0) and between +2.4V and +5V represents a logical high state (=1).

In order to permit communication to occur between host device 101 and peripheral device 107, interface circuit 100 further includes level shift/buffer 116 and universal asynchronous receiver/transmitter (UART) 118.

The role of level shift/buffer 116 is to perform level translation on the voltage signals being exchanged between host device 101 and peripheral device 107, such that voltage signals correlating to appropriate logic values are communicated between the devices. Thus, where a logical low (+0V) TTL signal is being transmitted from pin 112 of TTL peripheral device 107, level shift/buffer 116 converts this signal to the +12V logical low value understood by RS232 device 101. Conversely, where a logical high value of -12V is being transmitted from RS232 port 102, level shift/buffer 116 converts this signal to the +5V logical high value understood by TTL peripheral device 107. A level shift/buffer commonly employed for this purpose is National Semiconductor Corporation part No. DS14C535, which requires connection to power supplies of both the +5V and +12V variety.

The role played by UART 118 in permitting communication between the RS232 and non-RS232 devices two-fold.

5       UART 118 performs serial-to-parallel or  
parallel-to-serial conversion of signals exchanged  
between host RS232 device 101 and peripheral TTL  
device 107, such that each device receives a signal  
in the appropriate form. Thus UART 118 assembles a  
10       serial stream of one-bit signals transmitted from  
RS232 port 102, into discrete eight-bit words  
recognized at parallel port 109 by peripheral device  
107. Conversely, where an eight-bit data word is  
being transmitted in parallel form from pins 110 of  
peripheral device 107, UART 118 converts this  
15       parallel word into a serial stream of one-bit signals  
recognized at RS232 port 102 of host device 101. A  
UART commonly employed for use in interface  
applications is National Semiconductor Corporation  
part No. PC16550D.

20       The second function performed by UART 118 is to  
coordinate timing of transmission of the serial  
stream of electrical signals between the devices.  
Upon receiving a START bit from a transmitting  
device, UART 118 synchronizes receipt of the serial  
25       data stream at regular, predetermined intervals,  
enabling the serial data to be properly recognized.

While the conventional communication interface  
circuit shown in FIG. 1 is suitable for some  
applications, it suffers from a number of  
30       disadvantages. One disadvantage is a high part  
count. Specifically, the conventional interface  
circuit requires separate level shift/buffer and UART  
components described above. These components each  
contribute expense and complexity to the interface

circuit. Another disadvantage of the conventional circuit is that the level/shift buffer component must be connected with power supplies of both devices in order to perform level translation. A further  
 5 disadvantage is that the UART component is typically bulky and consumes precious space on the circuit board.

Therefore, there is a need in the art for a compact, simple, and inexpensive communication  
 10 interface circuit between devices utilizing different logic families which does not require separate components to perform level translation and parallel/serial conversion.

#### SUMMARY OF THE INVENTION

15 The present invention is a communications interface circuit enabling communication between devices utilizing dissimilar logic families, without requiring level translation. Proper conversion of the voltage level of exchanged signals is  
 20 accomplished by interposing a switching transistor between the two devices.

Taking advantage of a receiver threshold value of a first device, selective activation of the switching transistor permits a voltage signal in  
 25 excess of the receiver threshold voltage to be transmitted from a second device to the first device. This voltage signal is interpreted by the first device as the correct logic level.

In another aspect of the present invention, the  
 30 first device transmits a default voltage from the transmit pin while receiving a voltage on the receiver pin. Taking advantage of this property, selective deactivation of the switching transistor

isolates the first device from the second device, permitting the default voltage signal output from the transmit data pin of the first device to be returned back to the receive data pin the same (first) device.

5           An apparatus including a communication interface circuit in accordance with a first embodiment of the present invention comprises a first device including a first receive data terminal, a first transmit data terminal, a first power supply terminal configured to  
10 convey a first power supply voltage, and a second power supply terminal configured to convey a second power supply voltage. A second device includes a third power supply terminal configured to bear a third power supply voltage different from the first  
15 power supply voltage, a fourth power supply terminal configured to bear a fourth power supply voltage different from the second power supply voltage, a second receive data terminal configured to convey a received data signal, and a second transmit data  
20 terminal configured to convey a default voltage while the second receive data terminal receives a data signal. The second device interprets the received data signal traversing a receiver threshold value as a first logic state and interpreting the received  
25 data signal not traversing the receiver threshold value as a second logic state opposite the first logic state, the first power supply voltage traversing the receiver threshold value. A switch includes a first node, a second node, and a control  
30 node. The first node is in electrical communication with the first transmit data terminal, the second transmit data terminal, and the second receive data terminal. The second node is in electrical communication with the first power supply terminal,

and the control node in electrical communication with the first receive data terminal. The switch is configured to a first state to convey the first power supply voltage to the second receive data terminal, and the switch is configured to a second state to convey the default voltage signal from the second transmit data terminal to the second receive data terminal, and to convey a voltage signal from the second transmit data terminal to the first receive data terminal.

A method in accordance with one embodiment of the present invention for communicating between a first device utilizing a first logic family and a second device utilizing a second logic family different from the first logic family comprises the steps of forming an electrical connection between a first node of a switch and a transmit data terminal of the first device. An electrical connection is formed between the first switch node and a transmit data terminal of the second device. An electrical connection is formed between the first switch node and a receive data terminal of the second device, and an electrical connection is formed between a second node of the switch and a power supply of the first device. An electrical connection is formed between a control node of the switch and a receive data terminal of the first device. A first power supply voltage is transmitted from the receive data terminal of the first device to the switch control node, such that the switch is placed into a first state and a second power supply voltage is conveyed from the transmit data terminal of the second device to the transmit data terminal of the first device. The first power supply voltage is transmitted from the

receive data terminal of the first device to the switch control node, such that the switch is placed into the first state and a third power supply voltage is conveyed from the transmit data terminal of the second device to the receive data terminal of the second device. A fourth power supply voltage is transmitted from the receive data pin of the first device to the switch control node, such that the switch is placed into a second state and the first power supply voltage is conveyed from the first device to the receive data pin of the second device, the second device interpreting the received first power supply voltage traversing a receiver threshold value as a first logic state.

The features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic diagram of a conventional communication interface circuit requiring level translation.

FIG. 2 shows a schematic diagram of a communications interface circuit in accordance with one embodiment of the present invention.

FIGS. 3A-3F show schematic diagrams illustrating operation of the circuit shown in FIG. 2.

FIGS. 4A-4B show voltage timing diagrams illustrating the voltage conversion performed by the interface circuit of FIG. 2.

FIG. 5 shows a schematic diagram of a

communications interface circuit in accordance with an alternative embodiment of the present invention.

#### DETAILED DESCRIPTION

The present invention describes an interface circuit permitting communication between devices utilizing dissimilar logic families, without requiring level translation. This is accomplished by interposing a switching transistor between the two devices.

FIG. 2 shows a schematic diagram of a one embodiment of a communications interface circuit in accordance with the present invention. Communication circuit 200 includes host device 201 including RS232 port 202 featuring TXD pin 204 and RXD pin 206. TXD pin 204 and RXD pin 206 emit and receive, respectively, voltage signals whereby voltages between +3V and +12V are interpreted to represent a logical low state (=0), and voltages between -3V and -12V are interpreted to represent a logical high state (=1).

TTL microcontroller 208 of peripheral device 207 features parallel port 209 including eight pins, only two of which are shown in FIG. 2 as TXD pin 212 and RXD pin 214. TXD pin 212 and RXD pin 214 are configured to emit and receive respectively, voltage signals whereby voltages between 0V and +0.8V are interpreted to represent a logical low state (=0), and voltages between +2.4V and +5V are interpreted to represent a logical high state (=1). RXD pin 214 is capable of being connected with power supply rail 224 through switch 213.

Microcontroller 208 of peripheral device 207 also includes diodes 215 at RXD pin 212 and TXD pin

214. Diodes 215 limit the voltage of electrical signals permitted to enter pins 212 and 214, protecting microcontroller 208 from damage in the event of exposure to excessively high input voltages.

5           Communication interface circuit 200 further includes PNP switching transistor 216. Base 216a of PNP switching transistor 216 is connected to RXD pin 214 of microcontroller 208 through first (10 K $\Omega$ ) resistor 220. First resistor 220 limits the amount  
10 of base current through transistor 216. Emitter 216b of PNP transistor 216 is connected to +5V power supply rail 224. Power supply rail 224 may, but need not be, the same power supply utilized by TTL microcontroller 208.

15           TXD pin 204 of RS232 device 202 is connected with collector 216c of PNP transistor 216 through second (1K $\Omega$ ) resistor 228. RXD pin 206 of RS232 port 202 is connected with collector 216c of PNP  
20 transistor 216 through third (1K $\Omega$ ) resistor 230. TXD pin 212 of microcontroller 207 is connected with collector 216c of PNP transistor 216 through fourth (47K $\Omega$ ) resistor 232. Resistors 228, 230, and 232 serve primarily as current limiting devices.

25           Operation of the communication interface circuit of FIG. 2 is illustrated in FIGS. 3A-3F. FIG. 3A shows that for peripheral device 207 to receive data from RS232 device 202, switch 213 is activated. This causes RXD pin 214 of microcontroller 208 to be  
30 coupled with power supply rail 224 via diode 215 and exhibit the logical high state of +5V, and PNP switching transistor 216 to be turned off.

As a result, FIG. 3B shows transmission of a +12V signal from TXD pin 204 of RS232 device 202, through second (1K $\Omega$ ) resistor 228 and fourth (47K $\Omega$ )

resistor 232 to TXD pin 212 of microcontroller 208. The polarity of the signal received at TXD pin 212 is automatically inverted by software controlling microcontroller 208, eliminating the need for a  
5 separate physical inverter.

Assuming that the voltage and current of the transmitted signal do not exceed the range permitted by resistors 228 and 232 and diodes 215, the +12V signal is clamped at approximately +5.7V by the upper  
10 internal diode 215. Similarly, a -12V signal is clamped at approximately -0.7V by the lower internal diode 215. While both of these voltages are technically outside the official TTL signal voltage ranges, they will be recognized correctly nonetheless  
15 since they still fall within the maximum and minimum voltage limits for TTL compatible devices. FIG. 4A shows the voltage traces generated during this signal transmission stage of operation.

Next, FIG. 3C shows transmission of a logical  
20 low (=0) signal from microcontroller 208 to RS232 device 202. This is accomplished by grounding RXD pin 214 of microcontroller 208, thereby turning on PNP transistor 216. FIG. 3D shows that under these conditions, current flows from power supply rail 224  
25 through switching transistor 216 and third resistor 230, to RXD pin 206 of RS232 device 202. Because the RS232 standard establishes a receiver threshold value of +3V calling for any received voltage in excess of +3V to be interpreted as a low logic value, the  
30 approximately +5V input signal received at RXD pin 206 is interpreted by RS232 device 202 as if it were a +12V (logical low) signal.

FIGS. 3E-3F shows transmission of a logical high (=1) signal from microcontroller 207 to RS232 device 202.

First, FIG. 3E shows activation of switch 213 placing RXD pin 214 of microcontroller 208 in communication with high voltage rail 224, such that PNP transistor 216 is deactivated and high voltage power supply rail 224 is isolated from RS232 port 202.

Next, FIG. 3E shows that because the RS232 standard requires TXD pin 204 to continuously emit a -12V voltage when RS232 device 202 is otherwise idle, the present invention returns this default -12V voltage back to RS232 device 202 at RXD pin 206 as though this signal were externally generated. The -12V signal received on RXD pin 206 is naturally interpreted by RS232 device 202 as a logical high (=1) value.

During the step of receiving a voltage signal as shown in FIGS. 3D and 3F, inversion of the voltage signal by the microcontroller software is not required. The logical low signal is transmitted as +5V and interpreted by the RS232 device as +12V. The logical high signal is transmitted as -12V and then returned unchanged to the RS232 device for interpretation.

FIG. 4B shows the voltage traces generated during receipt of signals by the RS232 device. Because of the reduced receiver threshold voltage required by the RS232 device to indicate a logical low state (+3V rather than the full +12V), the +5V signal received at the RXD pin of the RS232 device is interpreted as a logical low value. The unchanged

-12V signal returned to the RS232 device is simply interpreted as a logical high value.

The present invention offers a number of important advantages over conventional communication interface architectures. One important advantage is reduction in part count. The interface circuit in accordance with the present invention replaces two parts (the level shift/buffer and the UART) with a single switching transistor, a few resistors, and the microcontroller of the peripheral device.

To understand how the UART component is replaced by the present invention, recall that the primary function of the UART is to conduct serial-to-parallel or parallel-to-serial conversion and to synchronize the exchange of data between the RS232 (serial) port and the TTL (parallel) microcontroller port. Where conversion of voltage signals to conform to appropriate logic levels is performed in accordance with the present invention rather than by a separate level shift/buffer component, it is possible to program the microcontroller to perform the necessary synchronization and serial/parallel conversion.

For example, National Semiconductor Corporation part no. COP8SA is an economical 8-bit microcontroller designed for embedded applications. The COP8SA includes a pin addressable 8-bit parallel port. Where the present invention is being utilized to permit communication between an RS232 device and a COP8SA microcontroller, a simple software program accomplishes: 1) inversion of the signal received at the COP8SA RXD pin as described in connection with FIG. 3B; 2) serial-to-parallel conversion of signals received from the RS232 device; 3) parallel-to-serial conversion of signals transmitted to the RS232

device; and 4) synchronization of exchange of signals between the RS232 and non-RS232 devices. Programming the microcontroller to control synchronization is discussed in The Art of Electronics, Horowitz and Hill, (2nd. Ed. 1989), Cambridge University Press, pp. 984, hereby incorporated by reference.

A simple software program written for the COP8SA microcontroller is set forth in the SOURCE CODE APPENDIX attached at the end of this detailed description. The software program also controls output of signals at the pins of the parallel port of the microcontroller.

The part count reduction offered by the first embodiment of the interface circuit of in FIGS. 2-3F reduces bulk and significantly lowers the cost of the interface circuit. For example, a rough estimate of the cost of the conventional interface circuit shown in FIG. 1 is \$5.80 = \$3.00 (National Semiconductor UART PC16550D) + \$2.80 (National Semiconductor level shift/buffer DS14C535). By comparison, the cost of the transistor and resistors shown in FIG. 2 is about \$1.25, a savings of almost 80%.

Significantly, the transistor and resistors utilized in the present invention in place of the level shift/buffer can also be physically incorporated within the microcontroller without affecting its operation. In this manner, the present invention could be integrated directly into the microcontroller itself, eliminating the bulk of a separate component containing the switching transistor and resistors.

Another advantage of a communication interface circuit in accordance with the first embodiment of the present invention is elimination of an external

charge pump. Because the interface circuit utilizes the existing power supply of the microcontroller to accomplish voltage conversion, no separate voltage supply is required, and the complexity and cost of the device is further reduced.

Although the invention has so far been described in connection with one particular embodiment, it must be understood that the present invention should not be unduly limited to this specific example. Various modifications and alterations in the structure and process of the present invention will be apparent to those skilled in the art without departing from the scope of the present invention.

For example, while FIGS. 2 and 3A-3F depict an interface circuit controlled by a bipolar switching transistor, this is not required by the present invention. FIG. 5 shows a schematic diagram of a first alternative embodiment of a communications interface circuit in accordance with the present invention. Communication circuit 500 includes host device 501 including RS232 port 502 featuring TXD pin 504 and RXD pin 506. TXD pin 504 and RXD pin 506 emit and receive, respectively, voltage signals whereby voltages between +3V and +12V are interpreted to represent a logical low state (=0), and voltages between -3V and -12V are interpreted to represent a logical high state (=1).

TTL microcontroller 508 of peripheral device 507 features parallel port 509 including eight pins, only two of which are shown in FIG. 2 as TXD pin 512 and RXD pin 514. TXD pin 512 and RXD pin 514 are configured to emit and receive respectively, voltage signals whereby voltages between 0V and +0.8V are interpreted to represent a logical low state (=0),

and voltages between +2.4V and +5V are interpreted to represent a logical high state (=1). RXD pin 514 is capable of being connected with power supply rail 524 through switch 513.

5           Communication interface circuit 500 further includes PMOS switching transistor 516. Gate 516a of PMOS switching transistor 516 is connected to RXD pin 514 of microcontroller 508. Source 516b of PMOS transistor 516 is connected to +5V power supply rail 10 524. Power supply rail 524 may, but need not be, the same power supply utilized by TTL microcontroller 508.

15           TXD pin 504 of RS232 device 502 is connected with drain 516c of PMOS transistor 516. RXD pin 506 of RS232 port 202 is connected with drain 516c of PMOS transistor 516. TXD pin 512 of microcontroller 507 is connected with collector 516c of PMOS transistor 516.

20           Moreover, while the above discussion and figures describe a communication interface circuit between an RS232 port and a National Semiconductor COP8SA microcontroller featuring a pin-addressable parallel 8-bit port, the present invention is not limited to this specific configuration. A communication 25 interface circuit between an RS232 port and another type of microcontroller would also fall within the scope of the present invention. In such an alternative embodiment, the simple software program controlling inversion of received voltage signals and performing serial-to-parallel and parallel-to-serial 30 conversions would differ from the program specific to the COP8SA part and set forth in the SOURCE CODE APPENDIX. Moreover, while the port of the COP8SA is pin addressable, the present invention could also be

employed with a port addressable microcontroller in conjunction with the use of a mask function.

In a further alternative embodiment of the present invention wherein communication occurs  
 5 between serial ports of devices of dissimilar logic families, the serial/parallel conversion conventionally performed by the UART and replaced by the microcontroller in the first embodiment, is unnecessary. However, level translation would still  
 10 be performed by operation of the intervening switching transistor.

Furthermore, while the above discussion describes a communication circuit interposed between an RS232 device and a TTL device, the present  
 15 invention is not limited to this particular configuration.

In yet another alternative embodiment of the present invention, the principles employed above in FIGS. 2 and 3A-3F could also be utilized to permit  
 20 communication between an RS232 port and a microcontroller utilizing one of the reduced voltage TTL standards employed for portable devices. And where the power supply of the TTL microcontroller is below the +3V receiver threshold value established by  
 25 the RS232 standard, it is possible to utilize a variant of the RS232 standard to accomplish communication.

For example, one RS232 variant (known as International Telegraph and Telephone Consultative  
 30 Committee (CCITT) recommendation v.10) utilizes a receiver threshold value of +0.3V rather than +3V. Another variant (known as CCITT recommendation v.11) utilizes a threshold activation voltage of +0.2V rather than +3V. Communication between either of

these RS232 variants and a non-RS232 device having a low power supply rail would be possible as long as the power supply of the non-RS232 device is high enough to activate the switching transistor.

5           Finally, while the above discussion and figures describe an embodiment of an interface circuit between an RS232 device and a dissimilar peripheral, the present invention is not limited to an RS232 device. Any device which 1) exhibits a receiver  
10           threshold value exceeded by the power supply of a second device, and which 2) transmits a default voltage during an idle state which can be conveyed back to the receive data pin of the original device,  
15           is eligible for implementation of the apparatus and method in accordance with the present invention.

          Given the above description and the variety of embodiments described therein, it is intended that the following claims define the scope of the present invention, and that the devices and processes within  
20           the scope of these claims and their equivalents be covered hereby.